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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	:	JACK C. WYBENGA, et al
Serial No.	:	10/658,977
Filed	:	September 10, 2003
For	:	APPARATUS AND METHOD FOR PERFORMING HIGH-SPEED LOOKUPS IN A ROUTING TABLE
Group No.	:	2189
Examiner	:	Horace L. Flournoy

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Commissioner for Patents
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Sir:

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal. The review is requested for the reason(s) stated in the arguments below, demonstrating the clear legal and factual deficiency of the rejections of some or all claims.

Claims 1-22 were rejected as anticipated by Lipman et al. (USP 6,192,051, hereinafter "Lipman"). These rejections are traversed. Independent claims 1 and 11 each require "a first portion of said first received address accesses an address table in a first memory circuit and an output of said

first memory circuit accesses an address table in a second memory circuit". This feature is not taught or suggested by Lipman.

While Lipman's Figure 11 does show that IP address bits [31:16] provide the index of an entry in the level-1 tree 150 (col. 15, lines 59-61), the output "Next Tree Index" (the "NT pointer") is not used to "access[] an address table in a second memory circuit" where the second memory circuit is one of the "M pipelined memory circuits", as claimed in Claims 1 and 11. Instead, the NT pointer from the level-1 tree 150 is used as an index into the level-2 next tree table 152 of the forwarding table (col. 15, lines 65-67). That is, rather than being used to access the next memory circuit in a pipeline of memory circuits forming a trie table, it appears to be used for a separate lookup as an index in a forwarding table. The output of that forwarding table appears to be used as an offset index, added to T2 base, into the level-2 tree 154.

Figure 11 shows that the NT pointer from the level-1 tree 150 is used as an index into the level-2 next tree table 152 of the forwarding table (col. 15, lines 65-67), and nothing teaches or suggests that the forwarding table is an address table in a second memory circuit, as claimed. That is, rather than being used to access the next memory circuit in a pipeline of memory circuits forming a trie table, it appears to be used for a separate lookup as an index in a forwarding table. The output of that forwarding table appears to be used as an offset index, added to T2 base, into the level-2 tree 154.

Examiner Flournoy alleges that element 144 portion "128.63" satisfies the claimed "first portion of said first received address". On the contrary, Lipman describes that "A portion of the level 1 tree 140 is shown in FIG. 7, including locations 128.63 through 128.68." *Col. 10, lines 59-60.*

Applicant assumes that this is a typographic error in the patent, and the reference to "140" should be to "144".

Examiner Flournoy also alleges that Lipman's next tree table 152 is the claimed "address table in the second memory circuit". Of course, by combining element 144 from Figure 7 and element 152 of Figure 11, Examiner Flournoy has utterly failed to show that there are any pipelined memory circuits, a clear legal deficiency, as these two figures do not show any common elements interrelating. Figure 11 is describing a compressed tree, Figure 7 is describing an uncompressed tree, and these do not interrelate.

In fact, though Lipman shows multiple tables that point to each other, nothing in Lipman's description teaches or suggests a lookup circuit comprising "M pipelined memory circuits" as claimed. Examiner Flournoy's statement that "these memory circuits are 'pipelined' in that they each point to another circuit" is factually incorrect. Those of skill in the art recognize that a "pipeline" is a series of elements each connected so that the output of one element is an input of the next element. See, for example, Figure 3 of the present application, where the output of each pipelined SRAM is an input to the next one in series. Lipman does not appear to teach or suggest such a pipeline at all, much less pipelined memory circuits.

Examiner Flournoy refers to Lipman's Figure 7 for "pipelined memory circuits", but this figure shows a diagram of a data structure, not memory circuits. Lipman doesn't teach series connections or pipelining at all. Examiner Flournoy responds by saying that "any address lookup operation is a pipelined transaction". This statement is both incorrect and irrelevant. The claims require pipelined memory circuits storing a trie table. Lipman doesn't teach or suggest pipelined

memory circuits. Examiner Flournoy's response is essentially that he defines the trie table to be a set of memory circuits. Even if this were correct – and it is not – this interpretation would still not meet the claim limitations. Examiner Flournoy's analysis is factually deficient, and the conclusion is legally deficient.

Claim 21 requires that the output from the address table in the first memory circuit is a first address pointer that indexes a start of an address table in a second memory circuit. Claims 2 and 12 include similar limitations. These features are not taught or suggested by Lipman.

As described above, the output of the level-1 tree 150 (the NT pointer) is used as an index into the level-2 next tree table 152 of the forwarding table (col. 15, lines 65-67). Lipman also describes that the base of the level-2 next tree table 152 is pointed to by the level 2 pointer 218 from the level pointer block 210. As such, it is clear that the NT pointer does not index a start of the address table in the second memory circuit, as claimed. As such, it is clear that Lipman also does not teach or suggest the features of claims 2, 12, or independent claim 21. Claim 21 also requires M pipelined memory circuits, not taught or suggested by Lipman. Lipman similarly does not teach or suggest the features of dependent claim 22.

As described above, Examiner Flournoy's rejections of all claims are both legally and factually deficient, and it would therefore be inappropriate to put the Applicant to the time and expense of an appeal at this time.

Other distinctions exist, and these matters can be fully discussed on appeal, should that be necessary.

CONCLUSION

As a result of the foregoing, the Applicant asserts that the claims in the Application are in condition for allowance over all art of record, and respectfully requests this case be returned to the Examiner for allowance or, alternatively, further examination.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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